

INTERNATIONAL JOURNALS

- J51. A. N. Tallarico, S. Stoffels, N. Posthuma, **P. Magnone**, D. Marcon, S. Decoutere, E. Sangiorgi, C. Fiegna, “PBTI in GaN-HEMTs With p-Type Gate: Role of the Aluminum Content on ΔV_{TH} and Underlying Degradation Mechanisms”, *IEEE Transactions on Electron Devices*, vol. 65, no.1, pp. 38-44, 2018.
- J50. A. N. Tallarico, S. Reggiani, **P. Magnone**, G. Croce, R. Depetro, P. Gattari, E. Sangiorgi, C. Fiegna, “Investigation of the hot carrier degradation in power LDMOS transistors with customized thick oxide”, *Microelectronics Reliability*, vol. 76-77, pp. 475-479, 2017.
- J49. E. Acurio, F. Crupi, **P. Magnone**, L. Trojman, F. Iucolano, “Impact of AlN Layer Sandwiched between the GaN and the Al₂O₃ Layers on the Performance and Reliability of Recessed AlGaIn/GaN MOS-HEMTs”, *Microelectronic Engineering*, vol. 178, pp. 42-47, 2017.
- J48. T. Caldognetto, L. Dalla Santa, **P. Magnone**, P. Mattavelli, “Power Electronics Based Active Load for Unintentional Islanding Testbenches”, *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3831 – 3839, 2017.
- J47. E. Acurio, F. Crupi, **P. Magnone**, L. Trojman, G. Meneghesso, F. Iucolano, “On Recoverable Behavior of PBTI in AlGaIn/GaN MOS-HEMT”, *Solide-State Electronics*, vol. 132, pp. 49-56, 2017.
- J46. **P. Magnone**, P. A. Traverso, C. Fiegna, “Experimental Technique for the Performance Evaluation and Optimization of 1/f Noise Spectrum Investigation in Electron Devices”, *Measurement*, vol. 98, pp. 421-428, 2017.
- J45. A. N. Tallarico, S. Stoffels, **P. Magnone**, N. Posthuma, E. Sangiorgi, S. Decoutere, C. Fiegna, “Investigation of the p-GaN Gate Breakdown in Forward-biased GaN-based Power HEMTs”, *IEEE Electron Device Letters*, vol. 38, no. 1, pp. 99-102, 2017.
- J44. A. N. Tallarico, **P. Magnone**, S. Stoffels, S. Lenci, J. Hu, D. Marcon, E. Sangiorgi, S. Decoutere, C. Fiegna “ON-State Degradation in AlGaIn/GaN-on-Silicon Schottky Barrier Diodes: Investigation of the Geometry Dependence”, *IEEE Transactions on Electron Devices*, vol. 63, no. 9, pp. 3479-3486, 2016.
- J43. F. Crupi, **P. Magnone**, S. Strangio, F. Iucolano, G. Meneghesso, “Low Frequency Noise and Gate Bias Instability in Normally OFF AlGaIn/GaN HEMTs”, *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 2219-2222, 2016.
- J42. A. N. Tallarico, S. Stoffels, **P. Magnone**, J. Hu, S. Lenci, D. Marcon, E. Sangiorgi, C. Fiegna, S. Decoutere, “Reliability of Au-free AlGaIn/GaN-on-Silicon Schottky Barrier Diodes under ON-State Stress”, *IEEE Transactions on Electron Devices*, vol. 63, no. 2, pp. 723-770, 2016.
- J41. M. Nicolai, M. Zanucoli, **P. Magnone**, D. Tonini, E. Sangiorgi, C. Fiegna, “Theoretical study of the impact of rear interface passivation on MWT silicon solar cells”, *Journal of Computational Electronics*, vol. 15, no. 1, pp. 277-286, 2016.
- J40. P. Procel, M. Zanucoli, V. Maccaronio, F. Crupi, G. Cocorullo, **P. Magnone**, C. Fiegna, “Numerical simulation of the impact of design parameters on the performance of back-contact back-junction solar cell”, *Journal of Computational Electronics*, vol. 15, no. 1, pp. 260-268, 2016.

- J39. M. Nicolai, M. Zanuccoli, **P. Magnone**, M. Galiazzo, D. Tonini, M. Bertazzo, E. Sangiorgi, C. Fiegna, "Simulation Study of Multi-wire front Contact Grids for Silicon Solar Cells", *Energy Procedia*, vol. 77, pp. 129–138, 2015.
- J38. M. Zanuccoli, **P. Magnone**, E. Sangiorgi, C. Fiegna, "Analysis of the Impact of Geometrical and Technological Parameters on Recombination Losses in Interdigitated Back-Contact Solar Cells", *Solar Energy*, vol. 116, pp. 37-44, 2015.
- J37. G. Paternoster, M. Zanuccoli, P. Bellutti, L. Ferrario, F. Ficorella, C. Fiegna, **P. Magnone**, F. Mattedi, E. Sangiorgi, "Fabrication, characterization and modeling of a silicon solar cell optimized for concentrated photovoltaic applications", *Solar Energy Materials and Solar Cells*, vol. 134, pp. 407-416, 2015.
- J36. **P. Magnone**, M. Debucquoy, D. Giaffreda, N. Posthuma, C. Fiegna, "Understanding the Influence of Busbars in Large-Area IBC Solar Cells by Distributed SPICE Simulations", *IEEE Journal of Photovoltaics*, vol. 5, no. 2, pp. 552-558, 2015.
- J35. A. N. Tallarico, **P. Magnone**, G. Barletta, A. Magri, E. Sangiorgi, C. Fiegna, "Influence of bias and temperature conditions on NBTI physical mechanisms in p-channel power U-MOSFETs", *Solide-State Electronics*, vol. 108, pp. 42-46, 2015.
- J34. P. Procel, V. Maccaronio, F. Crupi, G. Cocorullo, M. Zanuccoli, **P. Magnone**, C. Fiegna, "Analysis of the Impact of Doping Levels on Performance of back Contact-Back Junction Solar Cells", *Energy Procedia*, vol. 55, pp. 128-132, 2014.
- J33. D. Giaffreda, M. Debucquoy, **P. Magnone**, N. Posthuma, C. Fiegna "A Distributed Electrical Model for Interdigitated back Contact Silicon Solar Cells", *Energy Procedia*, vol. 55, pp. 71-76, 2014.
- J32. **P. Magnone**, R. De Rose, D. Tonini, M. Frei, M. Zanuccoli, A. Belli, M. Galiazzo, E. Sangiorgi, C. Fiegna, "Numerical Simulation on the Influence of Via and Rear Emitters in MWT Solar Cells", *IEEE Journal of Photovoltaics*, vol. 4, no. 4, pp. 1032-1039, 2014.
- J31. A. N. Tallarico, **P. Magnone**, G. Barletta, A. Magri, E. Sangiorgi, C. Fiegna, "Negative Bias Temperature Stress Reliability in Trench-Gated P-Channel Power MOSFETs", *IEEE Transactions on Device and Materials Reliability*, vol. 14, no. 2, pp. 657-663, 2014.
- J30. **P. Magnone**, P. A. Traverso, G. Barletta, C. Fiegna, "Experimental characterization of low-frequency noise in power MOSFETs for defectiveness modelling and technology assessment", *Measurement*, vol. 57, pp. 47-54, 2014.
- J29. D. Giaffreda, **P. Magnone**, M. Meneghini, M. Barbato, G. Meneghesso, E. Zanoni, E. Sangiorgi, C Fiegna, "Local Shunting in Multicrystalline Silicon Solar Cells: Distributed Electrical Simulations and Experiments", *IEEE Journal of Photovoltaics*, vol. 4, no. 1, pp. 40-47, 2014.
- J28. **P. Magnone**, D. Tonini, R. De Rose, M. Frei, F. Crupi, M. Lanuzza, E. Sangiorgi, C. Fiegna, "A Comparative Study of MWT Architectures by Means of Numerical Simulations", *Energy Procedia*, vol. 38, pp. 131–136, 2013.

- J27. **P. Magnone**, D. Tonini, R. De Rose, M. Frei, F. Crupi, E. Sangiorgi, C. Fiegna, "Numerical Simulation and Modeling of Resistive and Recombination Losses in MWT Solar Cells", *IEEE Journal of Photovoltaics*, vol. 3, no. 4, pp. 1215-1221, 2013
- J26. **P. Magnone**, C. Fiegna, G. Greco, G. Bazzano, S. Rinaudo, E. Sangiorgi "Numerical Simulation and Modeling of Thermal Transient in Silicon Power Devices", *Solid-State Electronics*, vol. 88, pp. 69-72, 2013.
- J25. R. De Rose, M. Zanucoli, **P. Magnone**, M. Frei, E. Sangiorgi, C. Fiegna, "Understanding the Impact of the Doping Profiles on Selective Emitter Solar Cell by Two-Dimensional Numerical Simulation", *IEEE Journal of Photovoltaics*, vol. 3, no. 1, pp. 159-167, 2013
- J24. R. De Rose, A. Malomo, **P. Magnone**, F. Crupi, G. Cellere, M. Martire, D. Tonini, E. Sangiorgi, "A methodology to account for the finger interruptions in solar cell performance", *Microelectronics Reliability*, vol. 52, no. 9-10, pp. 2500-2503, 2012.
- J23. **P. Magnone**, G. Napoletano, R. De Rose, F. Crupi, D. Tonini, G. Cellere, M. Galiazzo, E. Sangiorgi, C. Fiegna, "A Methodology to Account for the Finger Non-Uniformity in Photovoltaic Solar Cell", *Energy Procedia*, vol. 27, pp. 191-196, 2012.
- J22. F. Crupi, M. Alioto, J. Franco, **P. Magnone**, M. Togo, N. Horiguchi, G. Groeseneken, "Understanding the Basic Advantages of Bulk FinFETs for Sub- and Near-Threshold Logic Circuits From Device Measurements", *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 7, pp. 439-442, 2012.
- J21. **P. Magnone**, F. Crupi, N. Wils, H. P. Tuinhout, C. Fiegna, "Characterization and Modeling of Hot Carrier-Induced Variability in Subthreshold Region", *IEEE Transactions on Electron Devices*, vol. 59, no. 8, pp. 2093-2099, 2012.
- J20. M. Zanucoli, R. De Rose, **P. Magnone**, E. Sangiorgi, C. Fiegna, "Performance Analysis of Rear Point Contact Solar Cells by Three-Dimensional Numerical Simulation", *IEEE Transactions on Electron Devices*, vol. 59, no. 5, pp. 1311-1319, 2012.
- J19. F. Crupi, M. Alioto, J. Franco, **P. Magnone**, B. Kaczer, G. Groeseneken, J. Mitard, L. Witters, T. Y. Hoffmann, "Buried Silicon-Germanium pMOSFETs: Experimental Analysis in VLSI Logic Circuits Under Aggressive Voltage Scaling", *IEEE Transactions on Very Large Scale Integration Systems*, vol. 20, no. 8, pp. 1487-1495, 2012.
- J18. **P. Magnone**, F. Crupi, N. Wils, R. Jain, H. Tuinhout, P. Andricciola, G. Giusi, C. Fiegna, "Impact of Hot Carriers on nMOSFET variability in 45 nm and 65 nm CMOS Technologies", *IEEE Transactions on Electron Devices*, vol. 58, no. 8, pp. 2347-2353, 2011.
- J17. G. Giusi, F. Crupi, **P. Magnone**, "Criticisms on and comparison of experimental channel backscattering extraction methods", *Microelectronic Engineering*, vol. 88, no. 1, pp. 76-81, 2011.
- J16. **P. Magnone**, F. Crupi, M. Alioto, B. Kaczer, B. De Jaeger, "Understanding the potential and the limits of Germanium pMOSFETs for VLSI circuits from experimental measurements", *IEEE Transactions on Very Large Scale Integration Systems*, vol. 19, no. 9, pp. 1569-1582, 2011.

- J15. **P. Magnone**, F. Crupi, A. Mercha, P. Andricciola, H. Tuinhout, R. J. P. Lander, “FinFET mismatch in subthreshold region: theory and experiments”, *IEEE Transactions on Electron Devices*, vol. 57, no. 11, pp. 2848-2856, 2010.
- J14. G. Giusi, F. Crupi, C. Ciofi, C. Pace, **P. Magnone**, “Instrumentation design for cross-correlation measurements between gate and drain low frequency noise in MOSFETs”, *Fluctuation and Noise Letters*, vol. 9, no. 3, pp. 313-322, 2010.
- J13. S. Chabukswar, D. Maji, C.R. Manoj, K.G. Anil, V. Ramgopal Rao, F. Crupi, **P. Magnone**, G. Giusi, C.Pace, N. Collaert, “Implications of fin width scaling on variability and reliability of high-k metal gate finFETs”, *Microelectronic Engineering*, vol. 87, no. 10, pp. 1963-1967, 2010.
- J12. **P. Magnone**, A. Mercha, V. Subramanian, P. Parvais, N. Collaert, M. Dehan, S. Decouter, G. Groeseneken, J. Benson, T. Merelle, R. Lander, F. Crupi, C. Pace, “Matching performance of finFET devices with fin widths down to 10nm”, *IEEE Electron Device Letters*, vol. 30, no. 12, pp.1374-1376, 2009.
- J11. F. Crupi, G. Giusi, G. Iannaccone, **P. Magnone**, C. Pace, E. Simoen, C. Claeys, “Analytical model for the 1/f noise in the tunneling current through metal-oxide-semiconductor structures”, *Journal of Applied Physics* vol. 106, no. 7, 2009.
- J10. (*Invited*) **P. Magnone**, F. Crupi, G. Giusi, C. Pace, E. Simoen, C. Claeys, L. Pantisano, D. Maji, V. Ramgopal Rao, P. Srinivasan “1/f noise in drain and gate current of MOSFETs with high-k gate stacks”, *IEEE Transactions on Device and Materials Reliability*, vol. 9, no. 2, pp. 180-189, 2009.
- J9. D. Maji, F. Crupi, E. Amat, E. Simoen, B. De Jaeger, D.P. Brunco, C.R. Manoj, V. Ramgopal Rao, **P. Magnone**, G. Giusi, C. Pace, L. Pantisano, J. Mitard, R. Rodriguez, M. Nafria, “Understanding and Optimization of Hot Carrier Reliability in Germanium-on-Silicon pMOSFETs”, *IEEE Transactions on Electron Devices*, vol. 56, no. 5, pp. 1063-1069, 2009
- J8. G. Giusi, F. Crupi, C. Pace, **P. Magnone**, “Full Model and Characterization of Noise in Operational Amplifier”, *IEEE Transaction on Circuits and Systems I*, vol. 56, no. 1, pp. 97-102, 2009.
- J7. **P. Magnone**, L. Pantisano, F. Crupi, L. Trojman, C. Pace, G. Giusi, “On the impact of defects close to the gate electrode on the low frequency 1/f noise”, *IEEE Electron Device Letters*, vol. 29, no. 38, pp. 1056-1058, 2008.
- J6. **P. Magnone**, V. Subramanian, B. Parvais, A. Mercha, C. Pace, M. Dehan, S. Decoutere, G. Groeseneken, F. Crupi, S. Pierro, “Gate voltage and geometry dependence of the series resistance and of the carrier mobility in FinFET devices”, *Microelectronics Engineering*, vol. 85, no. 8, pp. 1728-1731, 2008.
- J5. F. Crupi, **P. Magnone**, A. Pugliese, G. Cappuccino, “Performance of Current Mirror with High-k Gate Dielectrics”, *Microelectronics Engineering*, vol. 85, no. 2, pp. 284-288, 2008.
- J4. **P. Magnone**, C. Pace, F. Crupi, G. Giusi, “Low Frequency Noise in nMOSFETs with subnanometer EOT Hafnium-based Gate Dielectrics”, *Microelectronics Reliability*, vol. 47, no. 12, pp. 2109-2113, 2007.

J3. P. Srinivasan, F. Crupi, E. Simoen, **P. Magnone**, C. Pace, D. Misra, C. Claeys, “Interfacial layer quality effects on low-frequency noise (1/f) in p-MOSFET with advanced gate stacks”, *Microelectronics Reliability*, vol. 47, no. 4-5, pp. 501-504, 2007.

J2. **P. Magnone**, F. Crupi, L. Pantisano, C. Pace, “Fermi-level pinning at polysilicon-HfO₂ interface as a source of drain and gate current 1/f noise”, *Appl. Phys. Lett.*, vol. 90, n. 7, 2007.

J1. F. Crupi, P. Srinivasan, **P. Magnone**, E. Simoen, C. Pace, D. Misra, C. Claeys, “Impact of the interfacial layer on low-frequency noise (1/f) behavior of MOSFETs with advanced gate stacks”, *IEEE Electron Device Letters*, vol. 27, no. 8, pp. 688-691, 2006.

INTERNATIONAL CONFERENCES

C43. A. N. Tallarico, S. Reggiani, **P. Magnone**, G. Croce, R. Depetro, P. Gattari, E. Sangiorgi, C. Fiegna, “Investigation of the hot carrier degradation in power LDMOS transistors with customized thick oxide”, *28th ESREF*, Bordeaux, France, 2017.

C42. G. Liu, T. Caldognetto, P. Mattavelli, **P. Magnone**, “Power-Based Droop Control Suppressing the Effect of Bus Voltage Ripples for DC Microgrids”, *ECCE*, Cincinnati, Ohio, USA, 2017.

C41. G. Liu, T. Caldognetto, P. Mattavelli, **P. Magnone**, “Power Sharing Analysis of Power-Based Droop Control for DC Microgrids Considering Cable Impedances”, *EPE*, Warsaw, Poland, 2017.

C40. A. Khodamoradi, G. Liu, P. Mattavelli, T. Caldognetto, **P. Magnone**, “On-Line Stability Monitoring for Power Converters in DC Microgrids”, *2nd ICDCM*, Nuremberg, Germany, 2017.

C39. E. Acurio, F. Crupi, **P. Magnone**, L. Trojman, F. Iucolano, “Impact of AlN Layer Sandwiched between the GaN and the Al₂O₃ Layers on the Performance and Reliability of Recessed AlGaN/GaN MOS-HEMTs”, *INFOS*, Potsdam, Germany, 2017

C38. T. Caldognetto, L. Dalla Santa, **P. Magnone**, P. Mattavelli, “Impedance Synthesis by Inverter Control for Active Loads in Anti-Islanding Testbenches”, *ECCE*, Milwaukee (WI), USA, 2016.

C37. L. Dalla Santa, T. Caldognetto, **P. Magnone**, P. Mattavelli, “Implementation of an Active RLC Load for Unintentional Islanding Test”, *EPE*, Karlsruhe, Germany, 2016.

C36. A. N. Tallarico, **P. Magnone**, S. Stoffels, S. Lenci, D. Marcon, E. Sangiorgi, S. Decoutere, C. Fiegna, “Understanding the Degradation Sources Under ON-state Stress in AlGaN/GaN-on-Si SBD: Investigation of the Anode-Cathode Spacing Length Dependence”, *IRPS*, Pasadena (CA), USA, 2016.

C35. M. Galiazzo, M. Bertazzo, T. Micheletti, M. Zanucoli, **P. Magnone**, “Technical and Economical Assessment on Wire Soldered Cell Metallization”, *EUPVSEC*, Hamburg, Germany, pp. 164-168, 2015.

C34. **P. Magnone**, D. Giaffreda, F. Ceccaroni, D. Tonini, M. Martire, M. Galiazzo, C. Fiegna, “Modeling of finger interruptions in PV solar cells by distributed circuit simulations”, *EUPVSEC*, Hamburg, Germany, pp. 848-851, 2015.

- C33. A. N. Tallarico, E. Sangiorgi, C. Fiegna, **P. Magnone**, G. Barletta, A. Magrì, “Modeling Spatial and Energy Oxide Trap Distribution Responsible for NBTI in p-Channel Power U-MOSFETs”, *27th ISPSD*, Hong Kong, pp. 153-156, 2015.
- C32. M. Nicolai, M Zanuccoli, **P. Magnone**, M. Galiazzo, D. Tonini, M. Bertazzo, E. Sangiorgi, C. Fiegna, “Simulation Study of Multi-wire Front Contact Grids for Silicon Solar Cells”, *5th SiliconPV*, Konstanz, Germany, 2015.
- C31. S. Strangio, **P. Magnone**, F. Crupi, C. Fiegna, C. Pace, G. Iannaccone, A. Heiman, D. Shamir, “Toward understanding of donor-traps-related dispersion phenomena on normally-ON AlGaIn/GaN HEMT through transient simulations”, *EUROSOI-ULIS*, pp. 217-220, Bologna, Italy, 2015.
- C30. A. N. Tallarico, **P. Magnone**, E. Sangiorgi, C. Fiegna, “Modeling Self-Heating Effects in AlGaIn/GaN Electronic Devices during Static and Dynamic Operation Mode”, *SISPAD*, pp. 233-236, Yokohama, Japan, 2014.
- C29. **P. Magnone**, P. A. Traverso, C. Fiegna, “Optimal Non-parametric Estimation of 1/f Noise Spectrum in Semiconductor Devices”, *19th Symposium IMEKO*, Benevento, Italy, 2014.
- C28. A. N. Tallarico, **P. Magnone**, G. Barletta, A. Magrì, E. Sangiorgi, C. Fiegna, “NBTI in p-channel power U-MOSFETs – Understanding the degradation and the recovery mechanisms”, *15th ULIS*, Stockholm, Sweden, 2014.
- C27. P. Procel, V. Maccaronio, F. Crupi, G. Cocorullo, M. Zanuccoli, **P. Magnone**, C. Fiegna, “Analysis of the Impact of Doping Levels on Performance of Back Contact - Back Junction Solar Cells”, *4th SiliconPV*, ‘s-Hertogenbosch, the Netherlands, 2014.
- C26. D. Giaffreda, M. Debucquoy, **P. Magnone**, N. Posthuma, C. Fiegna, “A Distributed Electrical Model for Interdigitated Back Contact Silicon Solar Cells”, *4th SiliconPV*, ‘s-Hertogenbosch, the Netherlands, 2014.
- C25. **P. Magnone**, G. Barletta, P.A. Traverso, A. Magrì, C. Fiegna, “Understanding Negative Bias Temperature Stress in p-Channel Trench Power MOSFETs by Low-Frequency Noise Measurement”, *26th ISPSD*, Waikoloa, USA, 2014
- C24. (*Invited*) **P. Magnone**, C. Fiegna, E. Sangiorgi, D. Tonini, M. Frei, “TCAD Numerical Simulation of Metal Wrap Through Solar Cell”, *EDSSC*, Hong Kong, 2013.
- C23. **P. Magnone**, P. A. Traverso, G. Barletta, C. Fiegna, "Low-Frequency Noise Measurements in Silicon Power MOSFETs as a Tool to Experimentally Investigate the Defectiveness of the Gate Oxide", *19th Symposium IMEKO*, Barcelona, Spain, 2013.
- C22. R. De Rose, **P. Magnone**, M. Zanuccoli, E. Sangiorgi, C. Fiegna, “Loss Analysis of Silicon Solar Cells by Means of Numerical Device Simulation”, *14th ULIS*, Warwick, UK, 2013.
- C21. **P. Magnone**, D. Tonini, R. De Rose, M. Frei, F. Crupi, M. Lanuzza, E. Sangiorgi, C. Fiegna, “A Comparative Study of MWT Architectures by Means of Numerical Simulations”, *3rd SiliconPV*, Hamelin, Germany, 2013.

- C20. (*Invited*) F. Crupi, **P. Magnone**, M. Alioto, J. Franco, G. Groeseneken, “Early Assessment of Emerging Technologies for VLSI Logic Circuits from Experimental Measurements”, *ICSICT*, Xi'an, China, 2012.
- C19. R. De Rose, A. Malomo, **P. Magnone**, F. Crupi, G. Cellere, M. Martire, D. Tonini, E. Sangiorgi, “A Methodology to Account for the Finger Interruptions in Solar Cell Performance”, *23rd ESREF*, Cagliari, Italy, 2012.
- C18. D. Giaffreda, **P. Magnone**, R. De Rose, M. Barbato, M. Meneghini, V. Giliberto, G. Meneghesso, E. Sangiorgi, C. Fiegna, “A Distributed Electrical Network to Model the Local Shunting in Multicrystalline Silicon Solar Cells”, *27th EU PVSEC*, Frankfurt, Germany, 2012.
- C17. G. Paternoster, **P. Magnone**, P. Bellutti, A. Collini, R. De Rose, L. Ferrario, F. Ficorella, C. Fiegna, F. Mattedi, E. Sangiorgi, M. Zanucoli “Silicon concentrator solar cells: fabrication, characterization and modeling for future improvements”, *27th EU PVSEC*, Frankfurt, Germany, 2012.
- C16. M. Barbato, M. Meneghini, V. Giliberto, D. Giaffreda, **P. Magnone**, R. De Rose, C. Fiegna, G. Meneghesso, “Effect of shunt resistance on the performance of mc-Silicon solar cells: a combined electro-optical and thermal investigation”, *38th PVSC*, Austin, USA, 2012.
- C15. **P. Magnone**, G. Napoletano, R. De Rose, F. Crupi, D. Tonini, G. Cellere, M. Galiazzo, E. Sangiorgi, C. Fiegna “A Methodology to Account for the Finger non-Uniformity in Photovoltaic Solar Cell”, *2nd SiliconPV*, Leuven, Belgium, 2012
- C14. **P. Magnone**, C. Fiegna, G. Greco, G. Bazzano, S. Rinaudo, E. Sangiorgi “Numerical Simulation and Modeling of Thermal Transient in Silicon Power Devices”, *13th ULIS*, Grenoble, France, 2012.
- C13. M. Zanucoli, R. De Rose, **P. Magnone**, M. Frei, H.-W. Guo, M. Agrawal, E. Sangiorgi, C. Fiegna, “Numerical Simulation and Modeling of Rear Point Contact Solar Cells”, *37th PVSC*, Seattle, USA, 2011.
- C12. R. De Rose, M. Zanucoli, **P. Magnone**, D. Tonini, M. Galiazzo, G. Cellere, M. Frei, H.-W. Guo, C. Fiegna, E. Sangiorgi, “2-D Numerical Analysis of the Impact of the Highly-Doped Profile on Selective Emitter Solar Cell Performance”, *37th PVSC*, Seattle, USA, 2011.
- C11. **P. Magnone**, R. De Rose, M. Zanucoli, D. Tonini, M. Galiazzo, G. Cellere, H.-W. Guo, M. Frei, E. Sangiorgi, C. Fiegna “Understanding the Impact of Double Screen-Printing on Silicon Solar Cells by 2-D Numerical Simulations”, *37th PVSC*, Seattle, USA, 2011.
- C10. R. De Rose, M. Zanucoli, **P. Magnone**, E. Sangiorgi, C. Fiegna, “Open Issues for the Numerical Simulation of Silicon Solar Cells”, *12th ULIS*, Cork, Ireland, 2011.
- C9. **P. Magnone**, C. Fiegna, G. Greco, G. Bazzano, E. Sangiorgi, S. Rinaudo, “Modeling of Thermal Network in Silicon Power MOSFETs”, *12th ULIS*, Cork, Ireland, 2011.
- C8. F. Crupi, M. Alioto, J. Franco, **P. Magnone**, B. Kaczer, G. Groeseneken, J. Mitard, L. Witters, T. Y. Hoffmann, “Experimental Analysis of Buried SiGe pMOSFETs from the Perspective of Aggressive Voltage Scaling”, *ISCAS*, Rio de Janeiro, Brazil, 2011.
- C7. J. Miltard, L. Witters, M. Garcia Bardon, P. Christie, J. Franco, A. Mercha, **P. Magnone**, M. Alioto, F. Crupi, L.-A. Ragnarsson, A. Hikavy, B. Vincent, T. Chiarella, R. Loo, J. Tseng, S. Yamaguchi, S. Takeoka, W.-E. Wang, P. Absil, T. Hoffmann, “Sub-nm EOT high-mobility SiGe-

55% channel pFETs: delivering high performance at scaled VDD”, *IEDM*, San Francisco, USA, 2010.

C6. **P. Magnone**, F. Crupi, M. Alito, B. Kaczer, “Experimental Study of Leakage-Delay Trade-off in Germanium pMOSFETs for Logic Circuits”, *ISCAS*, Paris, France, 2010.

C5. D. Maji, F. Crupi, **P. Magnone**, G. Giusi, C. Pace, E. Simoen, V. Ramgopal Rao, “Characterization of Interface and Oxide Traps in Ge pMOSFETs based on DCIV Technique”, *IEDST*, Mumbai, India, 2009.

C4. F. Crupi, **P. Magnone**, E. Simoen, A. Mercha, L. Pantisano, G. Giusi, C. Pace, C. Claeys, “The role of the interfaces in the 1/f noise of MOSFETs with high-k gate stacks”, *Meeting of The Electrochemical Society*, San Francisco, USA, 2009.

C3. (*Invited*) F. Crupi, **P. Magnone**, G. Iannaccone, G. Giusi, C. Pace, E. Simoen, C. Claeys, “**Modeling the gate current 1/f noise and its application to advanced CMOS devices**”, *ICSICT*, Beijing, China, 2008.

C2. **P. Magnone**, C. Crupi, G. Iannaccone, G. Giusi, C. Pace, E. Simoen, C. Claeys, “**A model for MOS gate stack quality evaluation based on the gate current 1/f noise**”, *Proceedings of the 9th International Conference on Ultimate Integration on Silicon*, Udine, Italy, pp. 141-144, 2008.

C1. F. Crupi, P. Srinivasan, **P. Magnone**, E. Simoen, C. Pace, D. Misra, C. Claeys, “Impact of the interfacial layer on the low-frequency noise (1/f) behavior of MOSFETs with advanced gate stacks”, *WODIM*, Catania, Italy, 2006.

BOOK CHAPTERS

B1. E. Sangiorgi, M. Zanucoli, R. De Rose, **P. Magnone**, C. Fiegna “Two- and Three-Dimensional Numerical Simulation of Advanced Silicon Solar Cells”, In S. Luryi, J. Xu, A. Zaslavsky, *Future Trends in Microelectronics: Frontiers and Innovations*, pp. 210, Wiley-IEEE Press, 2013.